Amendments to Specification

Please replace the Abstract with the following amended Abstract:

The present invention ~~discloss~~ discloses an ALU (Arithmetic Logic Unit) that can be operated as an OR gate, an AND gate, an adder gate and an exclusive OR gate using a half adder that uses a superconductor rapid single flux quantum logic device. The ALU using a half adder includes a half adder using a superconductor rapid single flux quantum logic device as a logic circuit, and a switching unit that has input ports respectively connected to a sum output port and a carry output port of the half adder and is operated as an OR gate, an AND gate, an adder gate and an exclusive OR gate using output signals of the half adder. The switching unit includes a first switch having an input port connected to the sum output port of the half adder, a second switch having an input port connected to the carry output port of the half adder and an output port connected to an output port of the first switch, and a third switch having an input port connected to the carry output port of the half adder.